Method of manufacturing a semiconductor device and semiconductor device obtained with such a method

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The invention relates to a method of manufacturing a semiconductor device with a field effect transistor, in which method a semiconductor body of silicon is provided at a surface thereof with a source region and a drain region of a first conductivity type, which both are provided with extensions and with a channel region of a second conductivity type, opposite to the first conductivity type, between the source region and the drain region and with a gate region separated from the surface of the semiconductor body by a gate dielectric above the channel region, and wherein a pocket region of the second conductivity type and with a doping concentration higher than the doping concentration of the channel region is formed below the extensions, and wherein the pocket region is formed by implanting heavy ions in the semiconductor body, after which implantation a first annealing process is done at a moderate temperature and a second annealing process with a fast ramp-up is done at a higher temperature. Such a method is very suitable for making MOSFET (= Metal Oxide Semiconductor Field Effect Transistor) devices. In the future CMOS (=Complimentary MOS) technology the formation of so-called pocket implants will become very essential since they have influence on the ion current of the transistor.

A method as mentioned in the opening paragraph is known from US patent US 6,432,802 B1 that has been issued on August 13, 2002. Therein (see embodiment 1 described in columns 6 and 7) such a method is described in which shallow extensions of source and drain are formed by doping, in this case, n-type ions into a semiconductor body. In addition, a p-type pocket dopant layer is formed under the extensions by doping with heavy ions, in this case indium ions. Next, a first annealing process is applied at a low temperature between 400 and 550 degrees Celsius, thereby changing the amorphous layer, i.e. a layer with (heavy) crystal damage, in the semiconductor body into a crystalline layer. Thereafter a second annealing process is done in the form of an RTA (= Rapid Thermal Annealing) in which the semiconductor body is heated up to an elevated temperature between 950 and 1050 degrees Celsius. In this way the highly doped extensions and the pocket implanted region are annealed and diffused.